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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/933,492	08/20/2001	David R. Hembree	00-0625.1	6973

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/933,492	HEMBREE ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *52 - 62 and 70 - 77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *52 - 62 and 70 - 77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/19/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on July 19, 2006 has been received and entered in the case.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following limitation "the conductor having a pattern containing information from testing of the semiconductor components" must be shown or the features canceled from the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet"

pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The amendment filed August 8, 2005 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "the conductor having a pattern containing information from testing of the semiconductor components".

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 52, 56, 60 and 70 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

(A) In claims 52, 56, 60 and 70, the specification fails to describe the phrase "the conductor having a pattern containing information from testing of the semiconductor components". The final product of this invention clearly shows in Fig. 2J, Fig. 7, Fig. 7A, Fig. 7B and page 12, line 1 – page 13, line 32 that the conductors 22p or 22 are just normal wiring circuits which are formed by etching the redistribution layer 20 according to the data received from the digital data 36. Furthermore, the specification clearly discloses in page 12, lines 8 – 15 that the digital data 36 (i.e., software) contains digital data representing locations of the good components, the defective component and the component contacts not the conductor. Thus, the newly added phrase "the conductor having a pattern containing information from testing of the semiconductor components" in the claims 52, 56, 60 and 70 are not supported by the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 52 – 62 and 70 – 77 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 52, 56, 60 and 70, it is unclear what the applicant regards as:

(a) Regarding the limitation "a plurality of redistribution conductors... in electrical communication with the component contacts configured to repair the

defective component" how is the plurality of redistribution conductors configured to repair the defective component?

(b) Regarding the limitation "the conductor having a pattern containing information from testing of the semiconductor components ... for repairing the defective component" it is unclear how the pattern of a conductor contains **information from testing of the semiconductor components** ... when the conductor is nothing more than a metal wire and not software.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 52 – 62 and 70 – 77 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanizawa (U. S. Pat. No. 4,721,995).

Regarding claims 52, 60 and 70, as best as understood by the Examiner, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) a semiconductor component comprising:

- a substrate (semiconductor wafer 1 in Fig. 4 and column 4, line 67) comprising a plurality of semiconductor components (semiconductor IC blocks 2; column 5, lines 1 – 15), each component including a plurality of component contacts (4; column 5, line 16) and a plurality of integrated circuits (Integrated circuits in the blocks 2; column 5,

lines 16 – 27) in electrical communication (by using the element 112) with the component contacts (4; see Fig. 3(a)), the components including a plurality of good components (good components, i.e., A, B, C and the not hatched block 2 in Fig. 4) and at least one defective component (any hatched block 2, i.e., E; see Fig. 4 and column 5, lines 61 – 62)

- a metal redistribution layer (claim 70; the metal redistribution line 5; column 5, lines 28 – 31) on the substrate (1) comprising a plurality of redistribution conductors (6B; column 5, lines 47 and 48) configured to either repair, reconfigure, or electrically isolate the defective component, or to electrically connect multiple components in a cluster that excludes the defective component (claim 70; see Fig. 3(a), Fig. 6(b), column 5, line 62 – column 6, line 5), and to repair the defective component (column 5, line 62 – column 6, line 5), and to reconfigure the component contacts (by redistribution line 5) on the defective component (claim 60; Fig. 3(a), Fig. 6(b), column 5, line 62 – column 6, line 5).

Furthermore, the limitation "the conductor having a pattern containing information from testing of the semiconductor components ... for repairing the defective component" is functional or intended use language that does not differentiate the claimed structure over Tanizawa. Since the term "information" is defined as the locations (i.e., the good components, the defective component and the component contacts) and the patterned conductor of Tanizawa also represents the locations (i.e., the good components, the defective component and the component contacts), the patterned conductor of Tanizawa contains the information. Thus, Tanizawa meets the claim.

Regarding claim 53, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) the components including a second defective component (a second hatched block for the bad blocks 2; column 5, lines 61 and 62) and the conductors (6B) being configured to electrically isolate the second defective component (see e.g., Fig. 6(b) and column 6, lines 25 – 30. since the conductors 6B is electrically connected to the new chip 8 and not electrically connected to the bad chip 2, Tanizawa fully meets this limitation.).

Regarding claim 54, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) the components (2) including a second defective component (a second hatched block for the bad blocks 2) and the conductors (6B or 11B) being configured to reconfigure the component contacts (4) on the second defective component (see e.g., Fig. 6(b). Since the contacts 4 on the bad chip 2 are physically attached to the contacts 9 on the good chip 8 thru the good chip 8, the contacts 9 read as reconfigured contacts of the contacts 4. Thus, Tanizawa fully meets this limitation.).

Regarding claim 55, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) the components (2) including a second defective component (a second hatched block for the bad blocks 2) and the conductors being configured to electrically connect multiple components in a cluster (wafer level IC) that excludes the second defective component (see e.g., Fig. 6(a) and Fig. 6(b)).

Regarding claim 56, as best as understood by the Examiner, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) a semiconductor component comprising:

- a substrate (semiconductor wafer 1 in Fig. 4) comprising a plurality of components (semiconductor IC blocks 2), a plurality of component contacts (4);

- the components (2) including a plurality of good components (e.g., any one of the good elements 2) and at least one defective component (any hatched block 2, i.e., E; see Fig. 4 and column 5, lines 61 – 62) identified during a component testing process (testing process; column 5, lines 62 – 66);
- a plurality of redistribution conductors (6) on the components configured to electrically isolate the component contacts on the defective component (any hatched block 2, i.e., E; see e.g., Fig. 4) on the substrate during testing of the good components (see e.g., Fig. 6(b) and column 6, lines 25 – 30. since the conductors 6B is electrically connected to the new chip 8 and not electrically connected to the bad chip 2, Tanizawa fully meets this limitation.).

Furthermore, the limitation "the conductor having a pattern containing information from testing of the components representing locations of the good components, the defective component and the component contacts, and for electrically isolating the defective component" is functional or intended use language that does not differentiate the claimed structure over Tanizawa. Since the term "information from testing of the components" is defined as the locations of the good components, the defective component and the component contacts and the patterned conductor of Tanizawa represents the locations of the good components, the defective component and the component contacts, the patterned conductor of Tanizawa contains the information from testing of the components. Thus, Tanizawa meets the claim. Even further, the term "burn-in" testing is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See In re Thorp, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 57, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) a plurality of terminal contacting (the attaching materials between the elements 6B and 4) on the good components (good 2s, i.e., A – D, etc.) in the selected patterns in electrical communication with the conductors (e.g., 4).

Regarding claim 58, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) the conductors (6B) being configured to electrically connect a plurality of good components in a cluster (wafer level IC) that exclude the defective component (see e.g., Figs. 6(a) and 6(b)).

Regarding claim 59, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) the substrate (1) comprising a semiconductor wafer (1; column 4, line 67), and the components (2) comprising semiconductor dice or semiconductor packages (die-IC; column 6, lines 51 – 55).

Regarding claim 61, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) a plurality of terminal contacts (the attaching materials between the elements 6B and 4) on the good components (2) in electrical communication with the conductors (6B) and the component contacts (4; see e.g., Figs. 3(a) and 3(b)) on the good components.

Regarding claims 62 and 76, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) the substrate (1) comprising a semiconductor wafer (1) or portion thereof and the components (2) comprising a semiconductor dice (die-IC; column 6, lines 51 – 55).

Regarding claim 71, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) the good components include a plurality of terminal contacts (the attaching materials between the elements 6B and 4) in electrical communication with the component contacts on the good components (see e.g., Fig. 3(a)).

Regarding claim 72, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) the component contacts (4) comprising bond pads (column 5, line 16).

Regarding claim 73, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) the conductors (6B) on the good components have a fan out configuration (see e.g., Fig. 3(a)).

Regarding claim 74, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) the substrate (1) comprising a semiconductor wafer (column 4, line 67).

Regarding claim 75, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) a protective layer (5; column 5, lines 28 and 29) on the conductors (6B) on the good components.

Regarding claim 77, Tanizawa discloses in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) the components (2) including a second defective component (the second hatched block 2 in Fig. 4) and the conductors (6B) being configured to electrically isolate the second defective component (column 5, lines 62 – 66).

Response to Arguments

10. Applicant's arguments filed on July 19, 2006 have been fully considered but they are not persuasive.

On page 11, applicant argues, "Tanizawa et al. does not disclose or enable 'redistribution conductors having a pattern containing information from testing of the semiconductor components'." This is not persuasive because Tanizawa et al. clearly shows in e.g., Fig. 3(a), Fig. 3(b), Fig. 4 and Fig. 6(b) redistribution conductors (6) having a pattern (the pattern of the element 6) containing information from testing of the semiconductor components (since final product of the element 6 is electrically connecting only one good component to another good

component, i.e., the repair component 8, not electrically connecting to a bad component, the element 6 of Tanizawa et al. reads as "containing information from testing of the semiconductor components". Even if the element 6 is not optimized for this purpose.) Furthermore, applicant should note that a recitation of the intended use or functional of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use or function, then it meets the claim.

For the above reasons, the rejection is maintined.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

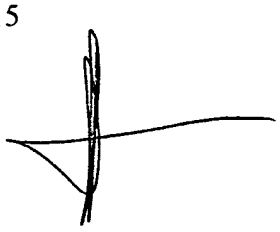
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Sunday, October 01, 2006



KENNETH PARKER
SUPERVISORY PATENT EXAMINER